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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 42390.P4918 Total Pages 5

First Named Inventor or Application Identifier Mohammad Abdallah

Express Mail Label No. EM501831839US

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. X Specification (Total Pages 22)
(preferred arrangement set forth below)
 - Descriptive Title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claims
 - Abstract of the Disclosure
3. X Drawings(s) (35 USC 113) (Total Sheets 7)
4. X Oath or Declaration (Total Pages 6)
 - a. Newly Executed (Original or Copy)
 - b. Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) (Note Box 5 below)
 - i. DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
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Respectfully submitted,

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Date: March 31, 1998

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Serial/Patent No.: _____ Filing/Issue Date: ***
Client: Intel Corporation
Title: SYSTEM AND METHOD FOR PERFORMING AN INSERT-EXTRACT INSTRUCTION

BSTZ File No.: 42390.P4918 Atty/Secty Initials: TAH/ldf
Date Mailed: 3/31/98 Docket Due Date: _____

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| <input type="checkbox"/> Appeal Brief (____ pgs.) (in triplicate) | <input type="checkbox"/> _____ Month(s) Extension of Time Amt: _____ |
| <input checked="" type="checkbox"/> Application - Utility (<u>22</u> pgs., with cover and abstract) | <input type="checkbox"/> Information Disclosure Statement & PTO 1449 (____ pgs.) <input checked="" type="checkbox"/> Check No. <u>21492</u> |
| <input type="checkbox"/> Application - Rule 1.60 Continuation (____ pgs.) | <input type="checkbox"/> Issue Fee Transmittal Amt: <u>\$1102.00</u> |
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| <input type="checkbox"/> Disclosure Doc. & Orig. & Copy of Inventor's Signed Paper (____ pgs.) | <input type="checkbox"/> Small Entity Declaration for Indep. Inventor/Small Business |
| <input checked="" type="checkbox"/> Drawings: <u>7</u> # of sheets includes <u>9</u> figures | <input checked="" type="checkbox"/> Transmittal Letter (original & copy) |

(Application & Fee Transmittals)

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FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT (\$) 1102.00

Complete if Known:

Application No. _____
Filing Date March 31, 1998
First Named Inventor Mohammad Abdallah
Group Art Unit _____
Examiner Name _____
Attorney Docket No. 42390.P4918

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:
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FEE CALCULATION (fees effective 10/01/97)

1. FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
101	790	201	395	Utility application filing fee	<u>790.00</u>
106	330	206	165	Design application filing fee	_____
107	540	207	270	Plant filing fee	_____
108	790	208	395	Reissue filing fee	_____
114	150	214	75	Provisional application filing fee	_____
SUBTOTAL (1)					\$ <u>790.00</u>

2. CLAIMS

					Extra		Fee from below		Fee Paid
Total Claims	<u>23</u>	-	<u>20</u>	=	<u>3</u>	X	<u>22.00</u>	=	<u>66.00</u>
Independent Claims	<u>6</u>	-	<u>3</u>	=	<u>3</u>	X	<u>82.00</u>	=	<u>246.00</u>
Multiple Dependent Claims						X		=	

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
103	22	203	11	Claims in excess of twenty	<u>66.00</u>
102	82	202	41	Independent claims in excess of 3	<u>246.00</u>
104	270	204	135	Multiple dependent claim	_____
109	82	209	41	Reissue independent claims over original patent	_____
110	22	210	11	Reissue claims in excess of 20 and over original patent	_____
SUBTOTAL (2)					\$ <u>312.00</u>

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	400	216	200	Extension for response within second month	
117	950	217	475	Extension for response within third month	
118	1,510	218	755	Extension for response within fourth month	
128	2,060	228	1,030	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,320	241	660	Petition to revive unintentionally abandoned application	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (see 37 CFR 1.129(a))	
Other fee (specify) _____					
Other fee (specify) _____					
SUBTOTAL (3)\$					0

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Thomas A. Hassing

Signature Thomas A. Hassing Date March 31, 1998

Reg. Number 36,159 Deposit Account User ID _____
(complete if applicable)

UNITED STATES PATENT APPLICATION

for

SYSTEM AND METHOD FOR PERFORMING AN INSERT-EXTRACT
INSTRUCTION

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Lisa Fluhr
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SYSTEM AND METHOD FOR PERFORMING AN INSERT-EXTRACT INSTRUCTION

FIELD OF THE INVENTION

5 The present invention relates in general to the field of computer systems, and in particular, to an apparatus and method for performing multi-dimensional computations based on an insert-extract operation.

BACKGROUND OF THE INVENTION

10 To improve the efficiency of multimedia applications, as well as other applications with similar characteristics, a Single Instruction, Multiple Data (SIMD) architecture has been implemented in computer systems to enable one instruction to operate on several operands simultaneously, rather than on a single operand. In particular, SIMD architectures take advantage of
15 packing many data elements within one register or memory location. With parallel hardware execution, multiple operations can be performed with one instruction, resulting in significant performance improvement.

 Although many applications currently in use can take advantage of such vertical operations, there are a number of important applications which
20 would require the rearrangement of the data elements before vertical operations can be implemented so as to provide realization of the application. Examples of such important applications include the dot product and matrix multiplication operations, which are commonly used in 3-D graphics and signal processing applications.

25 Therefore, there is a need for providing an apparatus and method for efficiently performing vertical SIMD computations.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and may be better understood by referring to the following description in conjunction with the accompanying drawings, in which like references indicate similar elements and in which:

FIG. 1 illustrates an exemplary computer system in accordance with one embodiment of the invention;

FIG. 2 illustrates the operation of the move instruction in accordance with one embodiment of the invention;

FIG. 3 illustrates the operation of the shuffle instruction in accordance with one embodiment of the invention;

FIG. 4 illustrates the operation of the inter-add instruction in accordance with one embodiment of the invention;

FIG. 5a and 5b illustrate the operation of the insert-extract instruction in accordance with one embodiment of the invention;

FIG. 6 illustrates the operation of the insert-extract instruction in accordance with one embodiment of the invention;

FIG. 7 is a general block diagram illustrating the usage of a digital filter which utilizes insert-extract operations, for filtering a TV broadcast signal in accordance with one embodiment of the invention;

FIG. 8 is a general block diagram illustrating the use of insert-extract operations, in rendering graphical objects in animation.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE PRESENT INVENTION

In the following description, numerous specific details are set forth to provide a thorough understanding of the invention. However, it will be understood by one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the invention.

According to one aspect of the invention, a method and apparatus are described for moving data elements into and out of a packed data operand (an insert-extract operation). The PINSRW and PEXTRW insert-extract instructions allow a user to insert or extract a word into or from any of the four 16-bit fields in a mm register or memory, which is 64 bits wide architecturally. The four fields consist of bits 63:48, 47:32, 31:16 and 15:0.

Because there are four fields to select from, the first two bits of an immediate field imm are used to designate which position to either insert the 16-bit word into a register or memory, or extract from the 64 bit word into the lower 16-bit word of a register or memory.

The term "registers" is used herein to refer to the on-board processor storage locations that are used as part of macro-instructions to identify operands. In other words, the registers referred to herein are those that are visible from the outside of the processor (from a programmers perspective). However, the registers described herein can be implemented by circuitry within a processor using any number of different techniques, such as dedicated physical registers, dynamically allocated physical registers using register renaming, combinations of dedicated and dynamically allocated physical registers, etc.

COMPUTER SYSTEM

FIG. 1 illustrates one embodiment of a computer system 100 which implements the principles of the present invention. Computer system 100 comprises a processor 105, a storage device 110, and a bus 115. The processor 105 is coupled to the storage device 110 by the bus 115. In addition, a number of user input/output devices, such as a keyboard 120 and a display 125, are also coupled to the bus 115. The processor 105 represents a central processing unit of any type of architecture, such as CISC, RISC, VLIW, or hybrid architecture. In addition, the processor 105 could be implemented on one or more chips. The storage device 110 represents one or more mechanisms for storing data. For example, the storage device 110 may include read only memory (ROM), random access memory (RAM), magnetic disk storage mediums, optical storage mediums, flash memory devices, and/or other machine-readable mediums. The bus 115 represents one or more buses (e.g., AGP, PCI, ISA, X-Bus, VESA, etc.) and bridges (also termed as bus controllers). While this embodiment is described in relation to a single processor computer system, the invention could be implemented in a multi-processor computer system. In addition, while this embodiment is described in relation to a 64-bit computer system, the invention is not limited to a 64-bit computer system.

In addition to other devices, one or more of a network 130, a TV broadcast signal receiver 131, a fax/modem 132, a digitizing unit 133, a sound unit 134, and a graphics unit 135 may optionally be coupled to bus 115. The network 130 and fax modem 132 represent one or more network connections for transmitting data over a machine readable media (e.g., carrier waves). The digitizing unit 133 represents one or more devices for digitizing images (i.e., a

scanner, camera, etc.). The sound unit 134 represents one or more devices for inputting and/or outputting sound (e.g., microphones, speakers, magnetic storage devices, optical storage devices, etc.). The graphics unit 135 represents one or more devices for generating 3-D images (e.g., graphics card).

5 FIG. 1 also illustrates that the storage device 110 has stored therein data 135 and software 136. Data 135 represents data stored in one or more of the formats described herein. Software 136 represents the necessary code for performing any and/or all of the techniques described with reference to FIG. 3-6. It will be recognized by one of ordinary skill in the art that the storage
10 device 110 preferably contains additional software (not shown), which is not necessary to understanding the invention.

 FIG. 1 additionally illustrates that the processor 105 includes decode unit 140, a set of registers 141, and execution unit 142, and an internal bus 143 for executing instructions. It will be recognized by one of ordinary skill in the
15 art that the processor 105 contains additional circuitry, which is not necessary to understanding the invention. The decode unit 140, registers 141 and execution unit 142 are coupled together by internal bus 143. The decode unit 140 is used for decoding instructions received by processor 105 into control signals and/or microcode entry points. In response to these control signals
20 and/or microcode entry points, the execution unit 142 performs the appropriate operations. The decode unit 140 may be implemented using any number of different mechanisms (e.g., a look-up table, a hardware implementation, a PLA, etc.). While the decoding of the various instructions is represented herein by a series of if/then statements, it is understood that
25 the execution of an instruction does not require a serial processing of these if/then statements. Rather, any mechanism for logically performing this

if/then processing is considered to be within the scope of the implementation of the invention.

The decode unit **140** is shown including packed data instruction set **145** for performing operations on packed data. In one embodiment, the packed data instruction set **145** includes the following instructions: a move instruction(s) **150**, a shuffle instruction(s) **155**, an add instruction(s) (such as ADDPS) **160**, and a multiply instruction(s) **165**. The MOVAPS, SHUFPS and ADDPS instructions are applicable to packed floating point data, in which the results of an operation between two sets of numbers having a predetermined number of bits, are stored in a register having the same predetermined number of bits, i.e., the size or configuration of the operand is the same as that of the result register. The operation of each of these instructions is further described herein. While one embodiment is described in which the packed data instructions operate on floating point data, alternative embodiments could alternatively or additionally have similar instructions that operate on integer data.

In addition to the packed data instructions, processor **105** can include new instructions and/or instructions similar to or the same as those found in existing general purpose processors. For example, in one embodiment the processor **105** supports an instruction set which is compatible with the Intel® Architecture instruction set used by existing processors, such as the Pentium® II processor. Alternative embodiments of the invention may contain more or less, as well as different, packed data instructions and still utilize the teachings of the invention.

The registers **141** represent a storage are on processor **105** for storing information, including control/status information, integer data, floating point data, and packed data. It will be understood by one of ordinary skill in

the art that one aspect of the invention is the described instruction set for operating on packed data. According to this aspect of the invention, the storage area used for storing the packed data is not critical. The term data processing system is used herein to refer to any machine for processing data, including the computer systems(s) described with reference to FIG. 1.

While one embodiment of the invention is described in which the processor 105, executing the packed data instructions operates on 128-bit packed data operands containing four 32-bit single precision floating point values, can operate on packed data in several different packed data formats.

For example, in one embodiment, packed data can be operated on in one of three formats: a "packed byte" format (e.g., PADDb), a "packed word" format (e.g., PADDw), or a "packed double word" (dword) format (e.g., PADDd). The packed byte format includes eight separate 8-bit data elements; the packed word format includes four separate 16-bit data elements; the packed dword format includes two separate 32-bit data elements 16-bit data elements. While certain instructions are discussed below with reference to one or two packed data formats, the instructions may be similarly applied the other packed data formats of the invention.

The shuffle instruction of the present invention is part of a family of many different instructions which operate with SIMD architecture. For example, FIG. 2 illustrates the operation of the move instruction 150 according to one embodiment of the invention. In this example, the move instruction 150 (MOVAPS) moves bits of data from one register to another register or from one memory location to another. In one embodiment, 64-bits representing four packed words from one memory location to another or from one register to another.

FIG. 3 illustrates the operation of the shuffle instruction 155 according to one embodiment of the invention. In one embodiment, the shuffle instruction 155 (SHUFPS) is able to shuffle any one of a plurality (e.g., four) single floating point (FP) numbers from a first operand 310 to the lower two destination fields of a destination register 330; the upper two destination fields are generated from a shuffle of any one of a plurality (e.g., four) single FP numbers from a second operand 320.

FIG. 4 illustrates the operation of the packed vertical add instruction 160 according to one embodiment of the invention. In one embodiment, the packed vertical operation is the add instruction (ADDPS) 160, which operates on the data elements of a first operand 410 and a second operand 420. In particular, the data elements of a first operand 410 are added to the respective packed data elements of a second operand 420, and are used to generate a result 430. For example, data element 0 of the first operand 410 is added to data element 0 of the second operand 420 and the result is stored as data element 0 of the result 430. The packed multiply instruction acts in a similar manner to the packed add instruction, except multiply operations are performed.

INSERT-EXTRACT OPERATIONS

FIG. 5a illustrates a technique for performing a PINSRW operation on two numbers according to one embodiment of the invention. In this application, data is represented by ovals, while instructions are represented by rectangles. Beginning from a start state, the process S500 proceeds to process step S510, where a number A is stored as a data element in a data item 515. For present discussion purposes, the data element is 16-bits wide.

The process S500 then proceeds to process step S520, where numbers B0, B1, B2 and B3 are stored as data elements in a packed data item 525. For present discussion purposes, each data element is 16-bits wide, and the operand to be inserted into is contained in register X, in the following order:

| B3 | B2 | B1 | B0 |

A 2-bit immediate value is used as a specifier field to indicate how data elements should be inserted. The two bits of the specifier field indicate which of the four data elements in the data operand are inserted into. For the purpose of explanation along with the example shown in FIG. 5a, an immediate value of 11 is used.

It will be recognized by one of ordinary skill in the art that the size of the insert specifier field may vary depending on the number of fields in the destination register. For example, with only a two field destination register, a one bit specifier field is sufficient to indicate how the data should be inserted.

The process S500 then advances to process step S530, where a PINSRW instruction is performed on the contents of the memory element (data item 515) and register X (data item 525) and immediate value 11, so as to replace data item B3 with A. The resulting data item 535 stored in register X is as follows:

| A | B2 | B1 | B0 |

Accordingly, a PINSRW operation is performed. Although FIG. 5a illustrates an example of the PINSRW operation with data operands having four data elements, the principles of the invention may also be implemented in data operands having at least two elements.

FIG. 5b illustrates a technique for performing a PEXTRW operation on two numbers according to one embodiment of the invention. Data is once again represented by ovals, while instructions are represented by rectangles.

Beginning from a start state, the process S540 proceeds to process step S550, where numbers B0, B1, B2 and B3 are stored as data elements in a packed data item 555. For present discussion purposes, each data element is 16-bits wide, and the operand to be inserted into is contained in register X, in the following order:

| B3 | B2 | B1 | B0 |

A 2-bit immediate value is used as a specifier field to indicate how data elements should be extracted. The two bits of the specifier field indicate which of the four data elements in the data operand are extracted from. For the purpose of explanation along with the example shown in FIG. 5b, an immediate value of 10 is used.

It will be recognized by one of ordinary skill in the art that the size of the extract specifier field may vary depending on the number of data elements in the source data operand. For example, with only a two element source register, a one bit specifier field is sufficient to indicate how the data should be extracted.

The process S500 then advances to process step S560, where a PEXTRW instruction is performed on the contents of register X (data item 555) and immediate value 10, so as to extract data item B2. The resulting data item 565 contains the value of B2.

Accordingly, a PEXTRW operation is performed. Although FIG. 5b illustrates an example of the PEXTRW operation with data operands having four data elements, the principles of the invention may also be implemented in data operands having at least two elements.

FIG. 6 illustrates a schematic for performing an insert operation on two numbers according to one embodiment of the invention. The device 611 takes the contents of a first source data operand 615 and a second source

packed data operand 613. A five to one data multiplexer 617 inserts any one of data elements {A} or {B3,B2,B1,B0} from either data operands 613, 615 into the first field of destination data item 625. A two to one data multiplexer 619 inserts either of data elements {A} or {B1} from either data operands 613, 615 into the second field of destination data item 625. A two to one data multiplexer 621 inserts either of data elements {A} or {B2} from either data operands 613, 615 into the third field of destination data item 625. A two to one data multiplexer 623 inserts either of data elements {A} or {B3} from either data operands 613, 615 into the fourth field of destination data item 625.

Accordingly, an insert operation is performed. Although FIG. 6 illustrates an example of the insert-extract operation with data operands having four data elements, the principles of the invention may also be implemented in data operands having at least two elements.

The insert-extract instruction of the present invention may be used as part of many different applications. For example, FIG. 7 is a general block diagram illustrating the use of a digital filter which utilizes an insert-extract operation for filtering a TV broadcast signal according to one embodiment of the invention. FIG. 7 shows TV broadcast signals 703 representing a television broadcast being received by a receiving unit 706 of a computer system 700. The receiving unit 706 receives the TV broadcast signals 703 and transforms them into digital data 709. A digital filter unit 715 performs a digital filter (e.g., FIR, IIR, etc.) on the digital data 709 using a set of coefficients 712. As a result, the digital filter unit 715 generates filtered data 718 (also termed as "filtered data items") representing the filtered analog TV broadcast signals. In performing the filtering operation, insert-extract operations is implemented. The filtered data 718 is received by a video decoder 721 for conversion into and audio & video data 724. The techniques performed by

video decoder 721 are well known (see Jack, Smith, Keith, "NTSC/PAL Digital Decoder", Video Demystified, High Text Publications, Inc., 1993) The audio and video data can be used for any purpose (e.g., display on a screen).

In one embodiment, the computer system 100 shown in FIG. 1 is used to implement the computer system 700 in FIG. 7. In this embodiment, the TV broadcast signal receiver 131 acts as the receiving unit 706 and may include a TV tuner, an analog to digital converter, and a DMA channel. The TV broadcast signals 703 are received by the TV tuner, converted into digital data by the analog to digital converter, and then sorted in the storage device 110 by the DMA channel. It will be recognized by one of ordinary skill in the art that the digital data sorted by the TV broadcast signal receiver 131 may be stored in any number of formats. For example, the TV broadcast signal receiver 131 may store the data in the main memory in one or more of the formats described herein - storing two representations of each of the components of the data such that it may be read in as packed data item in the described formats. This data may then be accessed as packed data and copied into registers on the processor 105. Since the data is stored in the disclosed formats, the processor 105 can easily and efficiently perform the insert-extract operation as described with reference to FIG. 5 and FIG. 6. It will be recognized by one of ordinary skill in the art that the receiving unit 706 may encompass additional hardware, software, and/or firmware in the TV broadcast signal receiver 131 or software executing on the processor 105. For example, additional software may be sorted in the storage device 110 for further processing the data prior to the digital filter being performed.

In this embodiment, the digital filter unit 718 is implemented using the processor 105 and the software 136 to perform the a digital filter. In this embodiment, the processor 105, executing the software 136, performs the

digital filter using insert-extract operations, and stores the filtered data 718 in storage device 110. In this manner, the digital filter is performed by the host processor of the computer system, rather than the TV broadcast signal receiver 131. As a result, the complexity of the TV broadcast signal receiver 131 is reduced. In this embodiment, the video decoder 721 may be implemented in any number of different combinations of hardware, software, and/or firmware. The audio and video data 724 can then be sorted, and/or displayed on the display 125 and the sound unit 134, respectively.

FIG. 8 is a general block diagram illustrating the use of an insert-extract operation for rendering graphical objects in animation according to one embodiment of the invention. FIG. 8 shows a computer system 800 containing digital data 755 representing 3-dimensional (3D) graphics. The digital data 810 may be stored on a CD ROM or other type of storage device for later use. At sometime, the conversion unit 760 performs alteration of data using 3D geometry which includes the use of an insert-extract operation to manipulate (e.g., scale, rotate, etc.) a 3D object in providing animation. The resulting graphical object 830 is then displayed on a screen display 840. The resulting graphical object may also be transmitted to a recording device (e.g., magnetic storage, such as tape).

In one embodiment, the computer system 100 shown in FIG. 1 is used to perform the 3D graphics operation 800 from FIG. 8. In this embodiment, the digital data 810 from FIG. 8 is any data stored in the storage device 110 representing 3D graphics. In one embodiment, the conversion unit 820 from FIG. 8 is implemented using the processor 105 and the software 136 to alter data using 3D geometry. An example of such alteration of data includes the performance of a 3D transformation. In this embodiment, the processor 105, executing the software 136, performs the transformation and stores the

transformed data 830 in the storage device 110 and/or provide, the transformed data to the graphics unit 135. In this manner, the 3D manipulation performed by the host processor of the computer system is provided at an increased speed. The present invention thus facilitates the performance of an insert-extract operation through the use of available instruction sequences.

While several examples uses of insert-extract operations have been described, it will be understood by one of ordinary skill in the art that the invention is not limited to these uses. In addition, while the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described. The method and apparatus of the invention can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting on the invention.

CLAIMS

What is claimed is:

1 1. A computer system comprising:
2 a hardware unit to transmit data representing graphics to another
3 computer or a display;
4 a processor coupled to the hardware unit; and
5 a storage device coupled to the processor and having stored therein a
6 routine, which when executing by the processor, causes the processor to
7 generate the data, the routine at least causing the processor to at least,
8 access a first data operand having a data element;
9 access a second packed data operand having at least two data
10 elements;
11 insert the data element in the first data operand into a
12 destination field of a destination register.

1 2. The computer system of claim 1 wherein the storage device further
2 comprises a packing device for packing floating point data into the data
3 elements.

1 3. The computer system of claim 1 wherein the storage device further
2 comprises a packing device for packing integer data into the data elements.

1 4. A computer system comprising:
2 a hardware unit to transmit data representing graphics to another
3 computer or a display;

4 a processor coupled to the hardware unit; and
5 a storage device coupled to the processor and having stored therein a
6 routine, which when executing by the processor, causes the processor to
7 generate the data, the routine at least causing the processor to at least,
8 access a first packed data operand having at least two data
9 elements; and
10 extract one of the data elements from the first packed data
11 operand into a field of a destination register.

1 5. The computer system of claim 4 wherein the storage device further
2 causes the processor to extract one of the data elements from the first packed
3 data operand into a field of a packed destination register.

1 6. The computer system of claim 4 wherein the storage device further
2 comprises a packing device for packing floating point data into the data
3 elements.

1 7. The computer system of claim 4 wherein the storage device further
2 comprises a packing device for packing integer data into the data elements.

1 8. A method comprising the computer-implemented steps of:
 2 decoding a single instruction;
 3 in response to the step of decoding the single instruction,
 4 accessing a first data operand having a data element;
 5 accessing a second packed data operand having at least two data
 6 elements;
 7 inserting the data element in the first data operand into a
 8 destination field of a destination register.

1 9. The method of claim 8 further comprising the step of packing floating
 2 point data into the data elements.

1 10. The method of claim 8 further comprising the step of packing integer
 2 data into the data elements.

1 11. A method comprising the computer-implemented steps of:
 2 decoding a single instruction;
 3 in response to the step of decoding the single instruction,
 4 accessing a first packed data operand having at least two data
 5 elements; and
 6 extracting one of the data elements from the first packed data
 7 operand into a field of a destination register.

1 12. The method of claim 11 wherein the step of extracting one of the data
 2 elements from the first packed operand comprises extracting one of the data
 3 elements from the first packed data operand into a field of a packed
 4 destination register.

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1 13. The method of claim 11 further comprising the step of packing floating
2 point data into the data elements.

1 14. The method of claim 11 further comprising the step of packing integer
2 data into the data elements.

1 15. A method comprising the computer implemented steps of:
2 accessing data representative of a first three-dimensional image;
3 altering the data using three-dimensional geometry to generate a
4 second three-dimensional image, the step of altering at least including,
5 accessing a first data operand having a data element;
6 accessing a second packed data operand having at least two data
7 elements;
8 inserting the data element in the first data operand into a destination
9 field of a destination register; and
10 displaying the second three-dimensional image.

1 16. The method of claim 15 wherein the step of altering includes the
2 performance of a three-dimensional transformation.

1 17. The method of claim 15 wherein the step of altering includes the step
2 of packing floating point data into the data elements.

1 18. The method of claim 15 wherein the step of altering includes the step
2 of packing integer data into the data elements.

1 19. A method comprising the computer implemented steps of:

2 accessing data representative of a first three-dimensional image;
3 altering the data using three-dimensional geometry to generate a
4 second three-dimensional image, the step of altering at least including,
5 accessing a first packed data operand having at least two data elements;
6 and
7 extracting one of the data elements from the first packed data operand
8 into a field of a destination register; and
9 displaying the second three-dimensional image.

1 **20.** The method of claim **19** wherein the step of altering further includes
2 the step of extracting one of the data elements from the first packed data
3 operand into a field of a packed destination register.

1 **21.** The method of claim **19** wherein the step of altering includes the
2 performance of a three-dimensional transformation.

1 **22.** The method of claim **19** wherein the step of altering includes the step
2 of packing floating point data into the data elements.

1 **23.** The method of claim **19** wherein the step of altering includes the step
2 of packing integer data into the data elements.

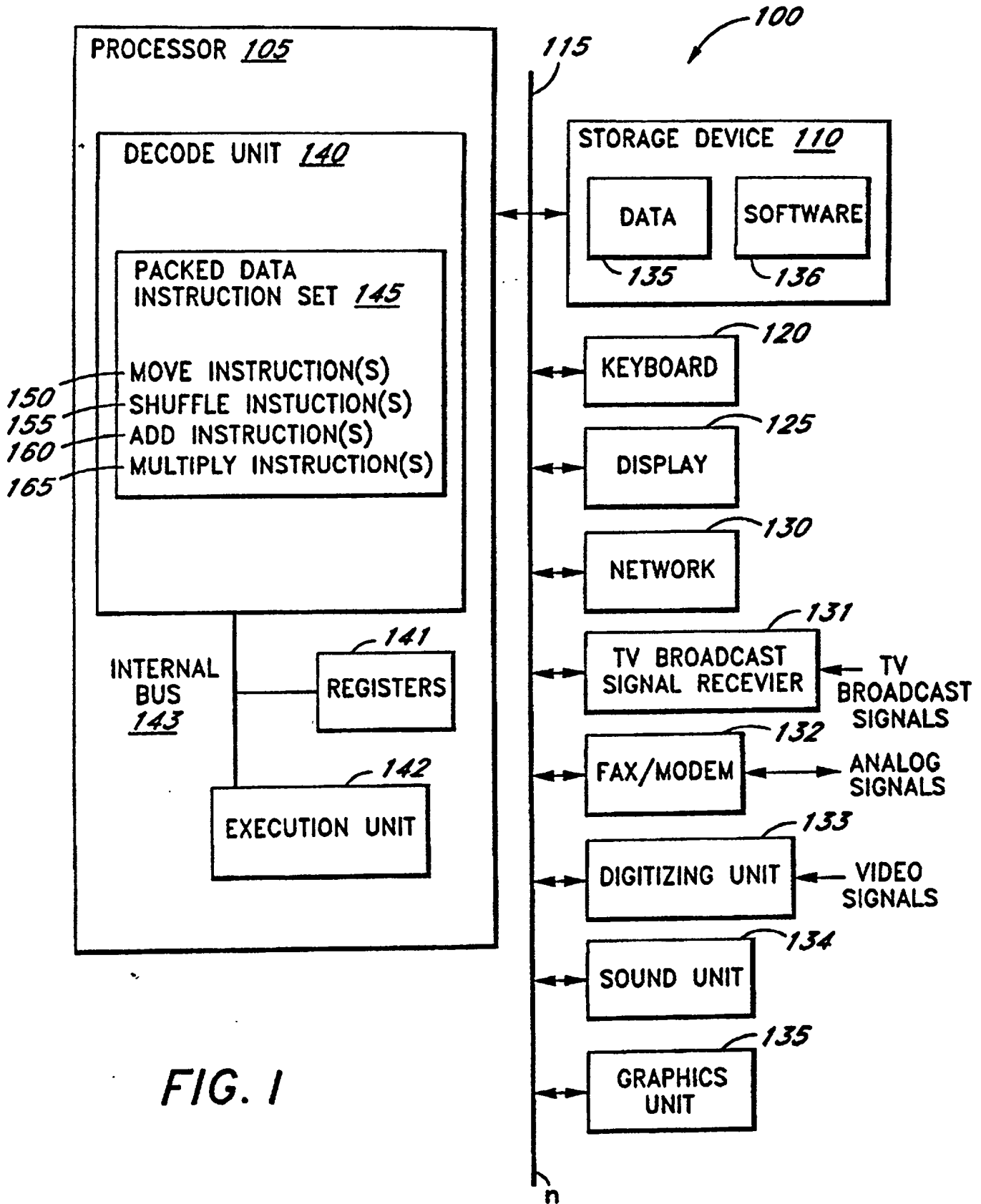


FIG. 1

FIG. 2

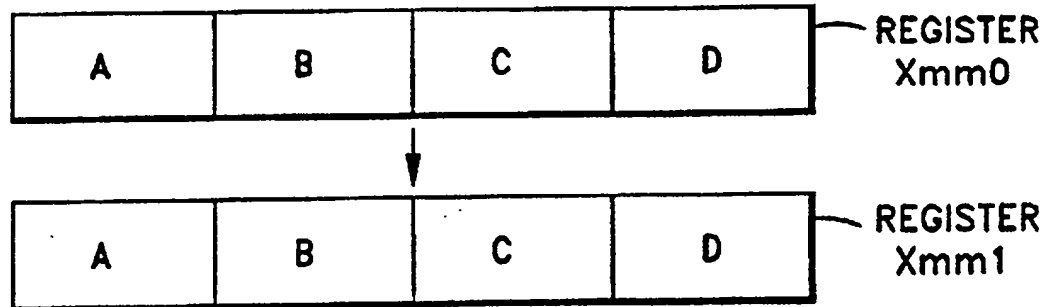


FIG. 3

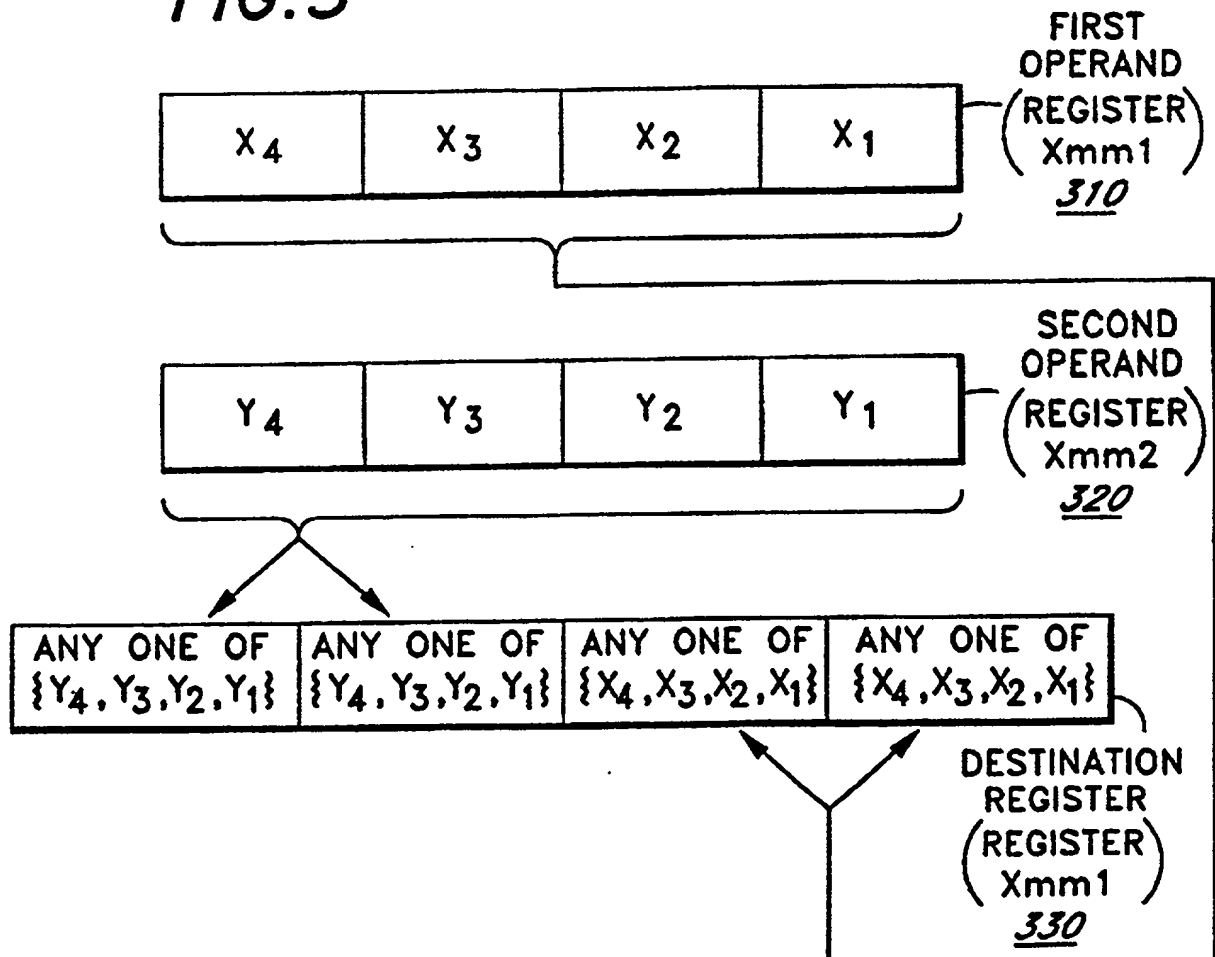


FIG. 4

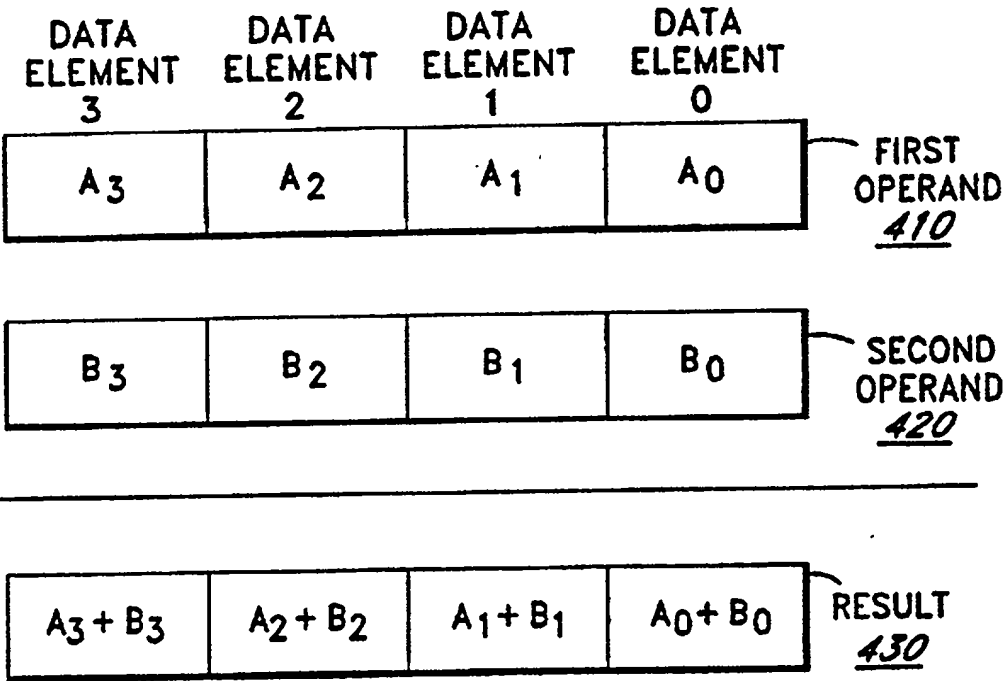


FIG. 5a

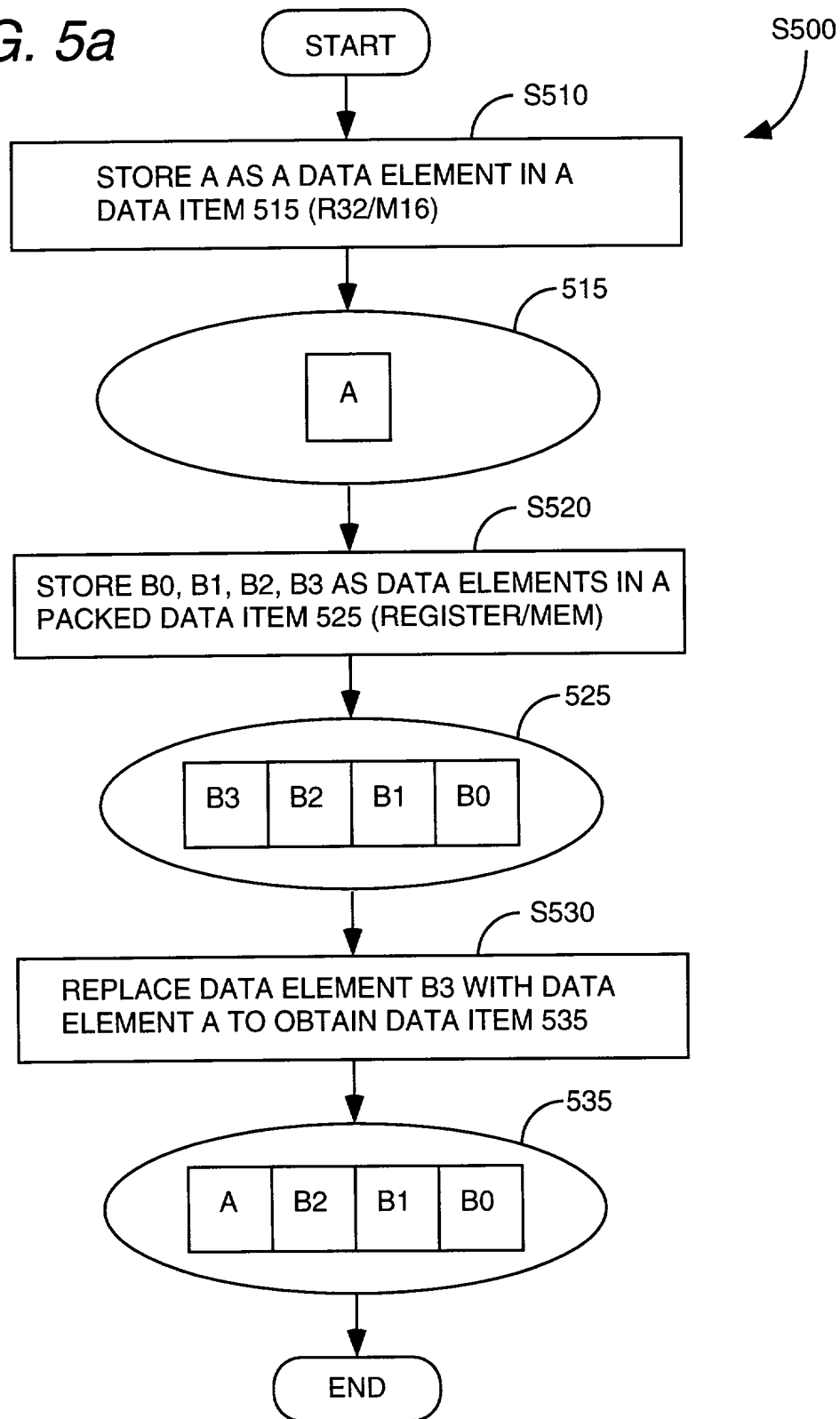
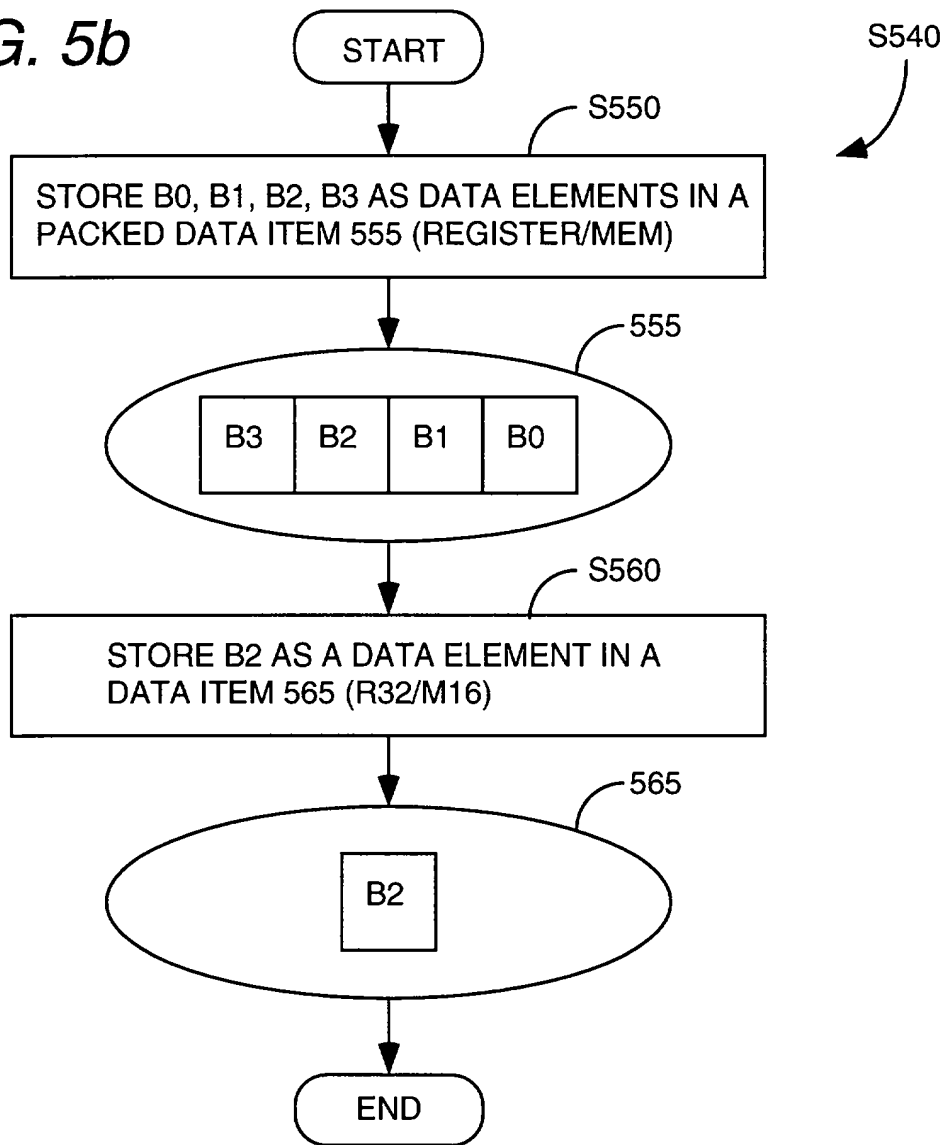


FIG. 5b



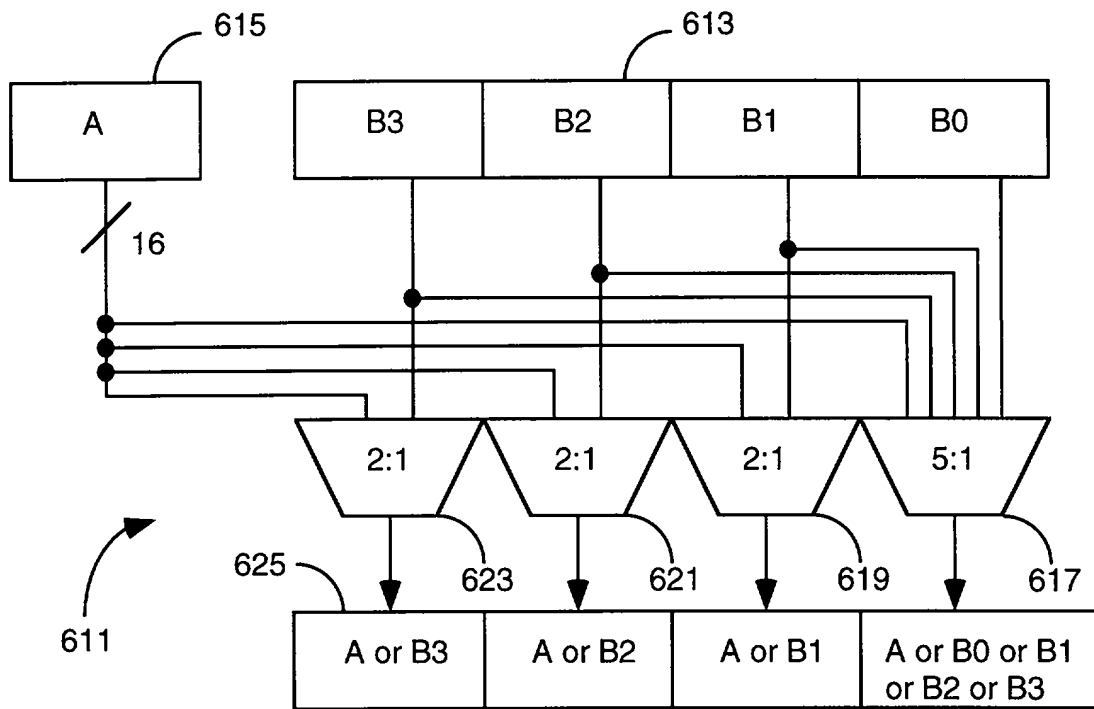


FIG. 6

FIG. 7

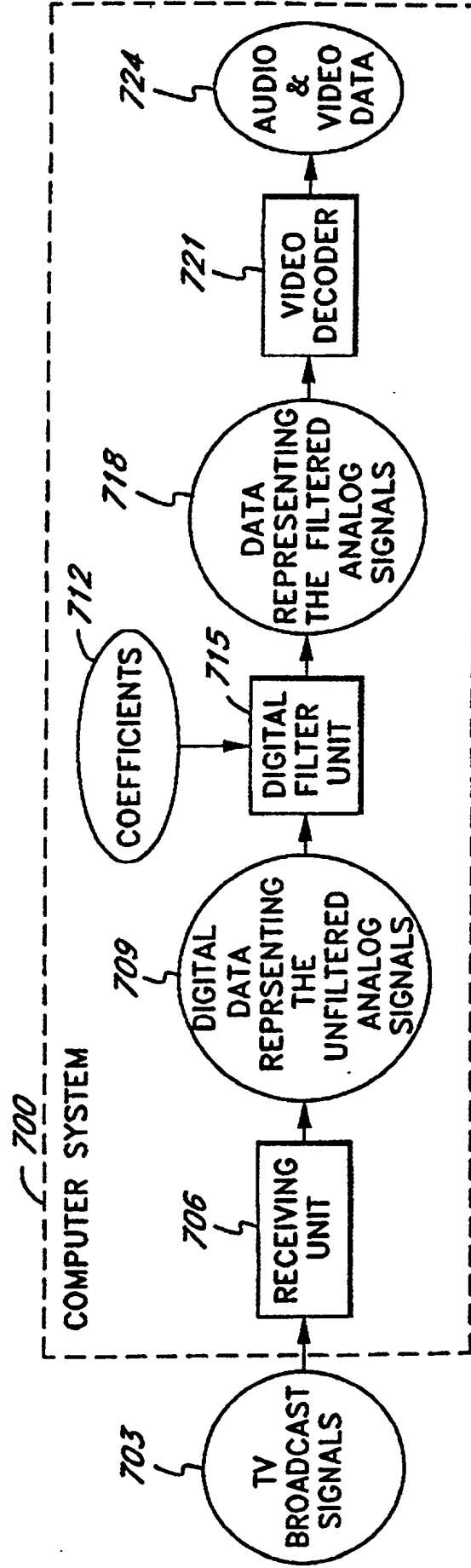
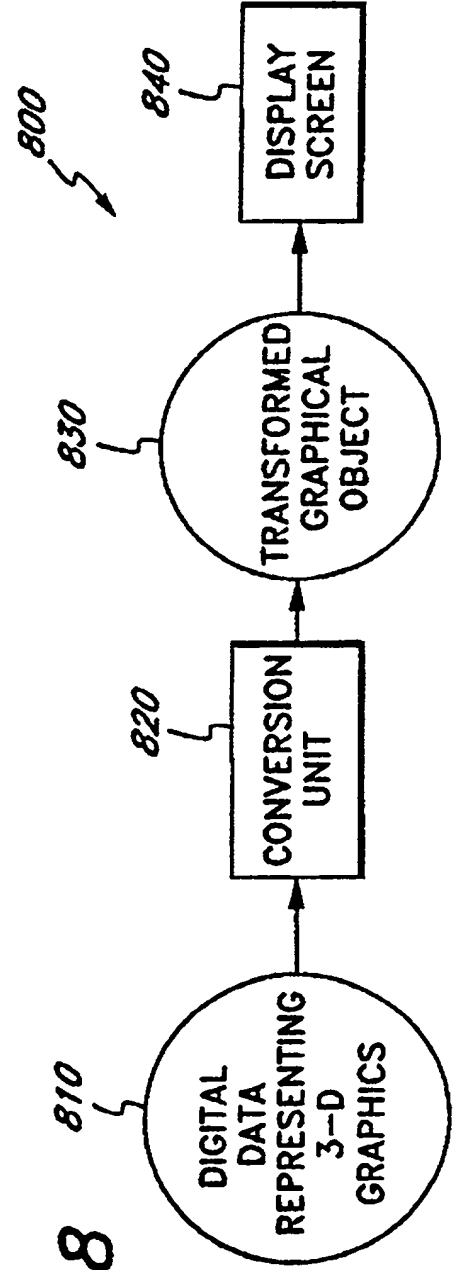


FIG. 8



Attorney's Docket No.: 42390.P4918

PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SYSTEM AND METHOD FOR PERFORMING AN INSERT-EXTRACT INSTRUCTION

the specification of which

XX is attached hereto.
_____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

[illegible]

(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

(Application Number)	Filing Date
(Application Number)	Filing Date

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

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(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and
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(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
- (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
- (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.